Influence of Surface Layers on the RF-Performance of AlInAs–GaInAs HFET's

J. Dickmann, H. Dämbkes, H. Nickel, R. Lösch, W. Schlapp, J. Böttcher, and H. Künzel

Abstract— **The influence of thickness and doping level of the GaInAs cap layer in AlInAs–GaInAs–InP HFET structures on the dc- and RF-performance is systematically investigated. We compare three different approaches, the undoped cap layer, the highly doped thick cap layer, and as a new approach, the thin doped and therefore surface depleted cap layer. HFET devices with 0.3 μm gates have been processed. While all devices demonstrate f_T-values around 80GHz distinct differences are observed for the $f_{\max}/f_T$ ratios between 1 (highly doped cap) over 1.3 (undoped cap) to 2.7 (surface depleted cap). The best $f_{\max}$ of 240 GHz is achieved for the new cap layer approach. A systematic investigation of the influence of the g_m/g_d and C_{gs}/C_{ds} ratios demonstrates the strong influence of a proper layout of the cap layer at the drain side of the gate region.**

I. Introduction

AlInAs–GaInAs HFET's grown on InP substrates have been demonstrated to be the best transistors for millimeter wave applications concerning lowest noise and highest cutoff frequencies [1]–[4]. Some properties like leakage currents, poor breakdown voltage and limited reliability still have to be improved. Attempts have been described to enhance the breakdown voltage and reduce the leakage current by use of thin undoped GaInAs cap layers [4], [6], [7] and/or especially tailored recess shapes [8]. These attempts however suffer from some parasitic resistances due to the undoped surface. In this contribution the best results are obtained in an approach combining the low resistance of the doped surface with high breakdown behavior of the surface depletion by use of a very thin highly doped cap layer that is just depleted by the surface potential. As a tool to investigate the extension of the depletion zone at the drain side of the gate with the electric field, the variation of C_{gd} with V_{GS} is measured and related to C_{gs}. While in the case of the highly doped cap layer the boundary of the depletion region is essentially pinned by the n^+-cap, resulting in a variation of C_{gd} with V_{DS} by a factor of two, the surface depleted structure allows for a wide movement of the depletion zone resulting in a variation by more than a factor of 5 and leading to the excellent cutoff frequency of 240 GHz for 0.3 μm devices. The reverse gate diode characteristics are clearly improved resulting in low leakage current and high breakdown voltage.

Manuscript received July 16, 1992. This work was supported by DBP-Telecom.

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IEEE Log Number 9204285.

II. Layer Sequence and Material Properties

Similar to our earlier work [5] the layer sequence was designed according to the following ideas: An undoped AlInAs buffer layer including a GaInAs–AlInAs superlattice at its both ends acts as trapping layer for contaminations and dopants from the substrate and to provide a high quality starting surface. On top of the second superlattice the undoped InGaAs channel is grown. So the superlattice provides an additional barrier to confine the carriers in the channel. On top of the channel layer a 2-nm undoped AlInAs spacer layer is followed by the actual carrier supply layer of Si-doped AlInAs with a doping thickness product of 5×10^{12} cm^{-2}. On top of the donor layer the 20-nm thick AlInAs Schottky layer is grown in order to enhance the gate diode barrier height and to reduce the gate leakage current. On top of this, a GaInAs cap layer is grown. For this investigation, the layer is either thick and highly doped (wafer A with 40 nm, 5×10^{18} cm^{-3}), or thin and moderately doped (wafer B 3 nm, 3×10^{18} cm^{-3}), or thin and undoped (wafer C 15 nm). All layers were grown by MBE in Varian systems. The growth temperature was kept constant around 500° C for sample B or varied between 480° C for GaInAs and 530° C for AlInAs (samples A, C). All samples show a carrier concentration in the 2 DEG of about 3×10^{12} cm^{-2} at 300 K and 2.7×10^{12} cm^{-2} at 77 K. The mobilities are between 8000 and 10 000 cm^2/Vs at 300 K and around 33 000 cm^2/Vs at 77 K. These data indicate the high quality of all the samples.

HFET's with 0.3-μm gate length and different width and shapes were fabricated as described in [9].

III. Device Performance

All devices were processed to result in threshold voltages around -1 V to -1.2 V. According to the different cap layers very different dc-results were achieved. The contact resistance was measured by TLM patterns: Due to the undoped cap the highest contact resistance of 0.40 hm/mm was measured in sample C. The lowest value was measured for the highly doped cap (A) with less than 0.10 ohm/mm. The influence of the parasitic resistance including the high sheet resistance of the undoped cap is clearly reflected in the output characteristics of the devices, also leading to a reduced extrinsic transconductance. For structure C, the transconductance was 380 mS/mm to 420 mS/mm while for structure B, a $g_{m\max}$ = 550 mS/mm was obtained. The saturation current for the

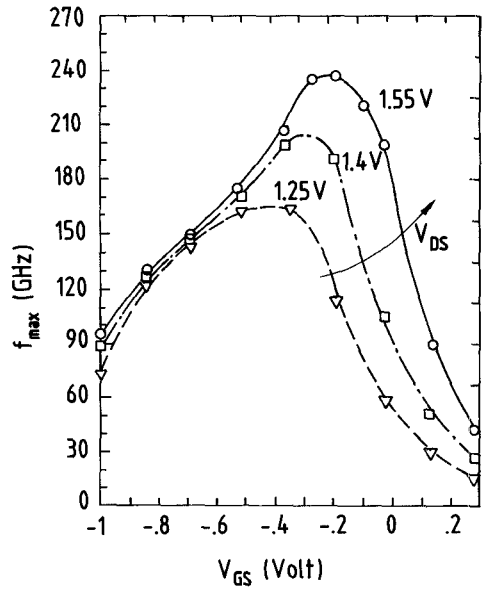

Fig. 1. $f_{\max}$ as a function of gate bias for the HFET device with depleted cap layer (sample B) $L = 0.3$ μm.

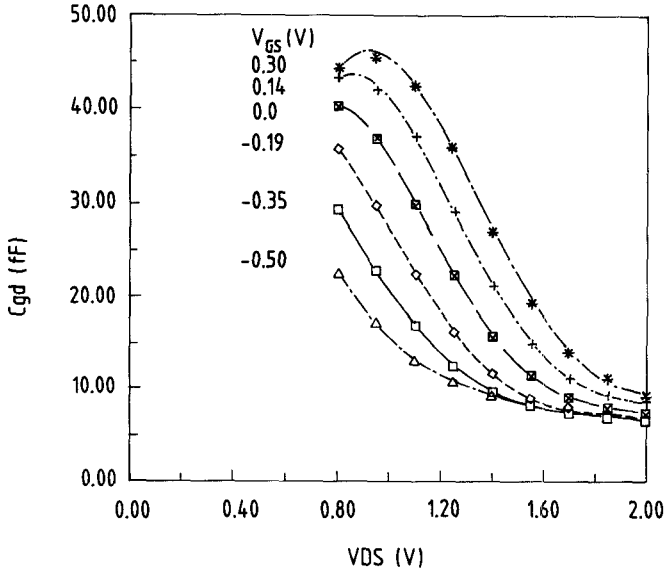

Fig. 2. f_T as a function of gate bias for the HFET device with depleted cap layer (sample B) $L = 0.3$ μm.

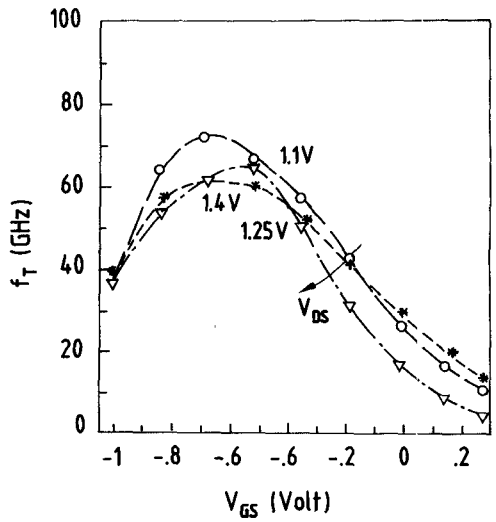

Fig. 3. Influence of bias on feedback capacitance C_{gd} for the device with depleted cap layer design (sample B) $W = 60$ m $L = 0.3$ μm.

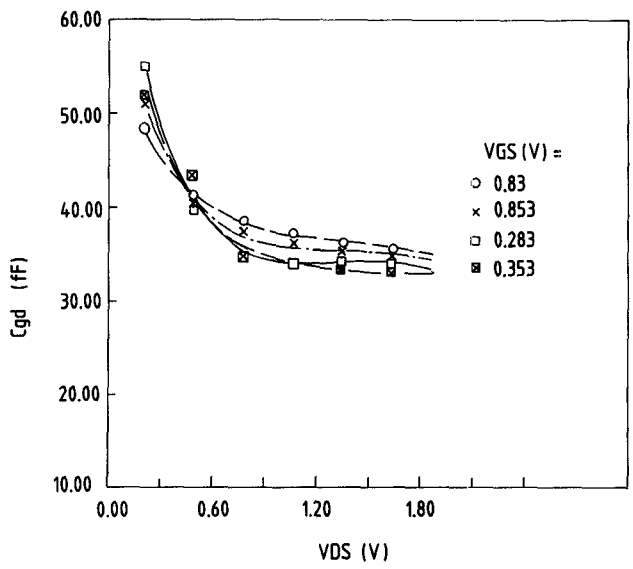

Fig. 4. Influence of bias on feedback capacitance C_{gd} for the device with highly doped cap layer design (sample A) $W = 60$ m $L = 0.3$ μm.

devices was between 400 mA/mm (structure C) and 600 mA/mm (structures B). The most significant difference is observed in the reverse gate characteristics and accordingly in the breakdown voltage. As shown in [9], a very low breakdown voltage and high leakage current is observed for structure A ($I > 25$ μA, $V_{GS} = -1$ V) while the two other characteristics are fully satisfying the device requirements. Remarkable is the result for structure B ($I < 5$ μA, $V_{GS} = -1$ V) with extremely low leakage currents.

The microwave properties of the transistors were measured using the coplanar on-wafer probing technique. The S-parameters were typically measured from 0.5–26.5 GHz and in some cases verified up to 40 GHz. From the measurements, the current gain cutoff frequency f_T and the unilateral gain cutoff frequency $f_{\max}$ were calculated. The MUG values were chosen because all devices had a stability factor far below 1. So MUG allows a comparison of performance by leading to $f_{\max}$ as figure of merit. The measured values of f_T for structure A, B, C are 90 GHz, 85 GHz, 75 GHz, and for $f_{\max}$ are 90 GHz, 240 GHz, 160 GHz, respectively. The calculated ratios $f_{\max}/f_T$ are for structure A, B, C are 1, 2.8, and 2.1, respectively.

The best result is clearly obtained for structure B with $f_{\max}$ = 240 GHz for L = 0.3 μm. This value is to our knowledge the best value reported for any material for this gate length.

IV. Bias Dependence and Analysis of Results

To gain better information about the different influences, all devices were fully characterized over a wide range of bias conditions. The gate voltage as well as the drain voltage was varied. For each bias point a full characterization including

determination of an equivalent small signal circuit was done and f_T and $f_{\max}$ were calculated. Figs. 1 and 2 show $f_{\max}$ and f_T values for sample B as a function of gate bias. Typical for InP HFET's is the distinct difference in the peak position: The maximum for f_T is obtained for small V_{DS}-values with a strongly pinched channel. The $f_{\max}$ values increase with increasing V_{DS} and the best value is obtain for full channel condition. The device performance does not improve towards higher values of V_{DS} for the devices shown. A more detailed analysis of this behavior is given in [10]. A clear influence of the surface layer type is observed in the size of C_{gd} and its dependence on bias condition. For this analysis, we determined small signal equivalent circuits for each bias point using the MicroCat optimizer for Cascade Microtech. While for sample B and the C_{gd} values are strongly influenced both by V_{gs} and V_{gd} (Fig. 3) C_{gd} for sample A is essentially controlled by V_{gs} (Fig. 4). The undoped cap of structure C allows for a large extension of the space charge region right from the start, sot he variation is only small and mainly controlled by V_{DS}. All this is explained by the distribution of the electric field at the drain edge of the recess area and its influence on the drift region of the electrons [6]. Here the new depleted cap layer approach (B) offers a good compromise to achieve low resistances as well as low feedback capacitances leading to excellent $f_{\max}$ values and a good $f_{\max}/f_T$ ratio.

V. Conclusion

We investigated the influence of the InGaAs cap layer design on the device performance of InAlAs–InGaAs HFET's. We were able to show, that designing the InGaAs cap layer as a surface depleted layer leads to improved gate leakage behavior and drastically improved values of $f_{\max}$. For an 0.3-μm gate length device a $f_{\max}/f_T$ of 240 GHz was determined.

Acknowledgment

The authors thank A. Wiersch for the RF measurements and software work.

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